adhesive material disposed between the upper surface of the wafer substrate and the lower surface of the glass sheet and affixing the glass sheet to the wafer substrate such that each hole in the glass sheet is aligned with an associated die bond pad formed in the upper surface of the integrated circuit die; and

for each solder ball bond pad, a strip of conductive material formed in electrical contact with said solder ball die bond pad and extending through the associated hole in the glass sheet and through the adhesive material to be electrically connected to the die bond pad associated with said hole; and

for each solder ball bond pad, a solder ball formed thereon to thereby provide an electrical connection between said solder ball and an associated die bond pad.

40. (New) A semiconductor integrated circuit structure as in claim 39, and wherein the glass sheet has a coefficient of thermal expansion that is substantially the same as the coefficient of thermal expansion of the wafer substrate.

41. (New) A semiconductor integrated circuit structure as in claim 40, and wherein the wafer substrate comprises silicon.

42. (New) A semiconductor integrated circuit structure as in claim 40, and wherein the integrated circuit structure further includes a pattern of wafer scribe lines formed therein such that the integrated circuit structure is disposed to be scribed along said scribe lines to provide a plurality of individual integrated circuit die, each said integrated circuit die having a scribed portion of said glass sheet affixed thereto.

43. (New) A semiconductor integrated circuit structure as in claim 40, and wherein the solder ball bond pads are a metal selected from the group consisting of aluminum, nickel, gold and copper.

44. (New) A semiconductor integrated circuit structure as in claim 40, and wherein

45. (New) A semiconductor integrated circuit structure as in claim 40, and wherein the strip of conductive material comprises a conductive polymer.

46. (New) A semiconductor integrated circuit structure as in claim 40, and further comprising:

a non-conductive mask formed on the upper surface of the glass sheet and patterned to facilitate formation of solder balls on the solder ball bond pads.

47. (New) A semiconductor integrated circuit structure comprising:

a semiconductor wafer substrate that includes a plurality of semiconductor integrated circuit die formed on an upper surface of the said wafer substrate;

for each semiconductor integrated circuit die, a plurality of conductive die bond pads formed on an upper surface of said integrated circuit die;

a glass sheet having a plurality of holes formed therethrough from an upper surface of the glass sheet to a lower surface of the glass sheet;

for each hole formed in the glass sheet, an associated conductive solder ball bond pad formed on the upper surface of the glass sheet in proximity to said hole and including a portion extending into said hole to cover sidewalls of said hole;

adhesive material disposed between the upper surface of the wafer substrate and the lower surface of the glass sheet and affixing the glass sheet to the wafer substrate such that each hole in the glass sheet is aligned with an associated die bond pad formed on the upper surface of the integrated circuit die; and

for each solder ball band pad, a conductive plug formed in the hole in the glass sheet associated with said solder ball bond pad and to be in electrical contact with the portion of said solder ball bond pad extending into said hole and also extending through the adhesive material to be in electrical contact with the die bond pad associated with said hole; and

for each solder ball bond pad, a solder ball formed thereon to thereby provide an electrical connection between said solder ball and on associated die bond pad.